**CSCE 312 – Lab 3 Report**

**Texas A&M University**

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**Poyi Ou­­­**

**Problem 1:**

1. D-Latch using NAND Gate

A diagram of a block diagram

Description automatically generated

1. D-Flip Flop using two D-Latch

A computer screen shot of a computer

Description automatically generated

**Problem 2:**

1. **Definition of SPST and NO in electro-mechanical switches**

SPST stands for Single Pole, Single Throw, representing a switch with two terminal connections: Normally Open (NO) and Common (C). The term 'Normally Open (NO)' indicates that in the resting state of the switch, there is no electrical connection between the Common (C) and Normally Open (NO) terminals. Therefore, when the SPST switch is activated, the circuit closes, allowing current to flow from the Common (C) terminal to the Normally Open (NO) terminal. Conversely, when the circuit is not activated, it remains open, creating an open circuit. The invention of the SPST switch has simplified design processes, made setups and wiring easier, and requiring less cabling.

1. **Digital Circuit Design**
   1. **Finite State Machine**

**A diagram of a number of circles and points

Description automatically generated**

* 1. **Truth Table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **S1** | **S0** | **B** | **LED** | **N1** | **N0** |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 1 |
|  |  |  |  |  |  |

* 1. **Equation**

LED = S1’S0B’+ S1’S0B + S1S0’B’ + S1S0’B

N1 = S1’S0B’+ S1S0’B’+ S1S0’B + S1S0B

N0 = S1’S0’B + S1’S0B + S1S0’B + S1S0B

1. **TTL ICs Used**

For the circuit I designed for this problem, I utilized 12 3-input AND gates, 3 4-input OR gates, and 3 NOT gates, which can be substituted with TTL-7408, TTL-7432, and TTL-7400, respectively.

**\***Note: We can recreate NOT gates by using the TTL-7400 2-input NAND gate and connecting the same wire to two different inputs.

1. **Final Circuit Designs**
   1. **Combinational Logic Design**

A diagram of a circuit

Description automatically generated

* 1. **Controller Circuit Design**

**A diagram of a computer

Description automatically generated**

**Problem 3:**

1. **Circuit Designs**
   1. **Truth table for Load Signals**

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **B2** | **B1** | **B0** | **I/O Enable** | **Head Light** | **D1** | **D2** | **D3** | **D4** | **Left Light** | **Right**  **Light** | **Wipers** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | **1** | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | **1** | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | **1** | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** |

\*B3 is not included, as when B3 is 0, the output remains unchanged.

* 1. **Simplified equation for the truth tables above:**

**Headlight** = B2’B1’B0’(I/O)

**D1** = B2’B1’B0(I/O)

**D2** = B2’B1B0’(I/O)

**D3** = B2’B1B0(I/O)

**D4** = B2B1’B0’(I/O)

**Left Light** = B2B1’B0(I/O)

**Right Light** = B2B1B0’(I/O)

**Wiper** = B2B1B0(I/O)

1. **Timing Diagram**

**A graph with lines on it

Description automatically generated with medium confidence**

1. **A diagram of a circuit

   Description automatically generatedCircuit Design Result**